Please amend the second full paragraph of page 44 as follows:

---After IC chip is mounted onto each of the printed circuit boards of the Examples and Comparative Examples, heat cycle tests of 1000 cycles and 2000 cycles under conditions of –55°C for 15 minutes, room temperature for 10 minutes and 125°C for 15 minutes are carried out.---

Please amend the fourth full paragraph of page 44 as follows:

---The results are shown in Table 1. As seen from the results of this table, the occurrence of cracks is not observed at about 1000 cycles in the Examples and Comparative Examples, while the occurrence of cracks is observed at 2000 cycles in the Comparative Examples. Further, the peel strength is equal or higher than that of the conductor circuit comprised of only an electroless plated film.---

IN THE ABSTRACT

Please use the Abstract attached to this response as the Abstract of the application.

IN THE CLAIMS

Please amend claims 1-4, 6, 7, 9, 11, 13, 14, 16, 18-23, and 29-43 as follows (a marked-up copy of changes to the claims is attached to the present amendment):

1. (Amended) A printed circuit board formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuit

is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer on at least a part of the surface of the conductor circuit.

2. (Amended) A printed circuit board formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer on at least a part of the surface of the conductor circuit, and the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal.

3. (Twice Amended) A printed circuit board according to claim 1, wherein the roughened layer is on at least a part of the surface inclusive of a side surface of the conductor circuit.

4. (Three Times Amended) A printed circuit board according to claim 1, wherein the roughened layer is on at least a part of a side face of the conductor circuit.

6. (Amended) A method of producing a multilayer printed circuit board comprising subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer.

7. (Amended) A method of producing a multilayer printed circuit board

comprising subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit, covering the surface of the roughened layer with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal and forming an interlaminar insulating layer.

9. (Amended) A multilayer printed circuit board comprising a substrate provided with an under layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, in which the viahole is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer having a roughened surface formed by etching treatment, polishing treatment, or redox treatment, or having a roughened surface formed by a plated film on at least a part of the surface of the underlayer conductor circuit connected to the viahole.

11.(Amended) A method of producing a multilayer printed circuit board comprising forming a lower conductor circuit layer on a surface of a substrate, forming a roughened layer by etching treatment, polishing treatment, redox treatment, or plating treatment on at least a part of the surface of the underlayer conductor circuit connected to a viahole, forming an interlaminar insulating layer thereon, forming openings for viaholes in the interlaminar insulating layer, subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon, subjecting the interlaminar insulating layer to an electrolytic plating, removing the plating resist, etching and

C 86 cont.

removing the electroless plated film beneath the plating resist to form an upperlayer conductor circuit comprised of the electroless plated film and the electrolytic plated film and a viahole.

Sub D4

13. (Amended) A printed circuit board provided with a conductor layer comprising an alignment mark, in which a roughened layer is formed on at least a part of the surface of the conductor layer.

C 87

14. (Amended) A printed circuit board provided with a conductor layer comprising an alignment mark, in which the conductor layer is comprised of an electroless plated film and an electrolytic plated film.

16. (Twice Amended) A printed circuit board according to claim 15, wherein a metal layer of nickel-gold is on the conductor layer exposed from the opening portion.

C 88

18. (Amended) A printed circuit board according to claim 14, wherein the roughened layer is on at least a part of the surface of the conductor layer.

C 89

19. (Twice Amended) A printed circuit board according to claim 13, which is made by a process comprising positioning a printed mask relative to the alignment mark.

20. (Twice Amended) A printed circuit board according to claim 13, which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

C 90

21. (Three Times Amended) A printed circuit board according to claim 13, which is made by a process comprising positioning a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

22. (Amended) A printed circuit board according to claim 2, wherein the roughened layer is on at least a part of the surface inclusive of a side surface of the conductor circuit.

C91

23. (Amended) A printed circuit board according to claim 2, wherein the roughened layer is on at least a part of a side face of the conductor circuit.

29. (Amended) A printed circuit board according to claim 14, which is made by a process comprising positioning a printed mask relative to the alignment mark.

30. (Amended) A printed circuit board according to claim 15, which is made by a process comprising positioning a printed mask relative to the alignment mark.

31. (Amended) A printed circuit board according to claim 16, which is made by a process comprising positioning a printed mask relative to the alignment mark.

C92

32. (Amended) A printed circuit board according to claim 17, which is made by a process comprising positioning a printed mask relative to the alignment mark.

33. (Amended) A printed circuit board according to claim 18, which is made by a process comprising positioning a printed mask relative to the alignment mark.

34. (Amended) A printed circuit board according to claim 14, which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

35. (Amended) A printed circuit board according to claim 15, which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

36. (Amended) A printed circuit board according to claim 16, which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

37. (Amended) A printed circuit board according to claim 17, which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

38. (Amended) A printed circuit board according to claim 18, which is made by a process comprising positioning an IC chip relative to the alignment mark during mounting.

39. (Amended) A printed circuit board according to claim 14, which is made by a process comprising positioning a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

C92 Cont.

40. (Amended) A printed circuit board according to claim 15, which is made by a process comprising positioning a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

41. (Amended) A printed circuit board according to claim 16, which is made by a process comprising positioning a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

42. (Amended) A printed circuit board according to claim 17, which is made by a process comprising positioning a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

43. (Amended) A printed circuit board according to claim 18, which is made by a process comprising positioning a printed circuit board packaged as a semiconductor element relative to the alignment mark during mounting to another printed circuit board.

Please add claims 44-49 as follows: